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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,027	09/30/2003	Dennis Kim	RAMB-01016US0	5412

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EXAMINER	
PANWALKAR, VINEETA S	

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,027	KIM ET AL.	
	Examiner	Art Unit	
	VINEETA S. PANWALKAR	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-8,10-24 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10,11 and 14-24* is/are allowed.

6)☒ Claim(s) *1,5,6,12,13 and 30* is/are rejected.

7)☒ Claim(s) *2,3,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. The indicated allowability of claims 1, 5, 6, 12 and 13 is withdrawn in view of the newly discovered references. Rejection(s) based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1, 5, 6 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over previously cited Beherns (US 5572558), hereinafter, Beherns in view of Heyne et al. (US 6285228 B1, hereinafter, Heyne) and Notani et al. (US 5592109, hereinafter, Heyne).

2a. Regarding claim 1, Beherns discloses a timing recovery phase locked loop (PLL) for synchronizing the sampling of a received signal wherein is disclosed a clock circuit comprising:

- a clock circuit (Fig. 3, unit 28) capable of generating a clock signal in response to a phase signal (VFO F50 provides a clock signal to the sampling device 24 based on the error signals provided by the phase and frequency error detectors F54 and F52) (See Fig.3 and column 8, lines 15-30); and
- a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate (The analog to digital converter (A/D) 24 is the claimed sampler. It receives the analog read signal 11. The data rate of the signal is varying. (Column 5, lines 1-23 explain how the data rate varies from track to track of the disk which stores the data). (See Fig.3 and column 8, lines 15-30).

Thus, Behrens discloses all the limitations, but fails to explicitly disclose whether the phase step size is adjustable and the claimed four stages with stall logic.

However, Heyne discloses a circuit comprising a clock circuit capable of generating a clock signal in response to an adjustable phase-step size (Column

2, lines 19-50; Fig. 4 and column 6, line 64-column 7, line 25. The phase regulator connected downstream of the phase detector generates an adjustable delay step using fine and coarse control signals and this is equivalent to claimed adjustable phase-step size).

It would have been obvious to a person of ordinary skill in the art to use adjustable phase step in a clock circuit as shown by Heyne because this allows for more accurate generation of clock signal.

Further, Notani discloses a clock circuit which includes at least four stages each having a respective stage output (Figs. 6 and 16, column 26, line 65 – column 27, line 32 and column 22, lines 33-45; wherein stages 18 and 20 from Fig. 6 are interpreted to be claimed first and second stages. Fig. 16 shows the outputs of the phase comparator of Fig. 6 being fed to flip flops 31 and 32 (claimed third and fourth stages). The outputs of the flip flops 31 and 32 are maintained (claimed holding) to be UPf and DOWNf in response to outputs UP and DOWN of the first two stages in the phase comparator. Thus, the claimed stall logic operation is performed by the circuit disclosed by Notani.).

Thus, it would have been obvious to a person of ordinary skill in the art to use the four stage structure in the clock circuit as disclosed by Notani because Notani's technique performs phase comparison at high speed with a simple structure and facilitates stability (Column 15, lines 43 -54).

2b. Regarding claim 5, Behrens, Heyne and Notani disclose all the limitations claimed.

Further, it is pointed out that no criticality is shown in choosing the claimed 6 pipeline stages. It appears as if the individual blocks of the circuit may process data within one or more stages, i.e. requiring one or more pipeline stages. Hence any 6 of Beherns' individual blocks such as the A/D 24, equalizer 26, detectors F54 ad F52, filter F56 and VFO F50 will inherently comprise at least 6 pipeline stages (See Fig.3 and column 8, lines 15-30).

2c. Regarding claim 6, Behrens, Heyne and Notani disclose all the limitations claimed.

Further, it is pointed out that no criticality is shown in choosing the claimed range of values (0 ppm –5000ppm). It appears as if the values have been chosen only as an example to demonstrate the variation in data rate. Hence the variation is data rate shown by Beherns reads on the claim (Column 5, lines 1-23 explain how the data rate varies from track to track of the disk which stores the data).

2d. Regarding claim 13, Behrens, Heyne and Notani disclose all the limitations claimed.

Further, Beherns further discloses the circuit wherein:

- the circuit is included in a receive circuit coupled to a transmit circuit capable of transmitting the data signal (Broadly speaking, Fig.1 shows a system wherein data is encoded using units 4,6,10 and 14 to form symbols 16 that are transmitted via magnetic recording channel 18 and received in order to be decoded. Fig.3 also shows the circuit that receives encoded data and performs timing recovery in the receiver).

3. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Beherns in view of Heyne and Notani as applied to claim 1 above, and further in view of previously cited Nakamura (US 20020030522 A1, hereinafter, Nakamura).

3a. Regarding claim 12, Behrens, Heyne and Notani disclose all the limitations claimed.

Further, Notani discloses the circuit wherein the clock circuit includes and a circuit with up and down signals and a filter capable of performing averaging (Fig. 5, unit 103), but fails to disclose whether plurality of up and down signals are averaged.

However, in the same field of endeavor, Nakamura shows a clock generator wherein

- the clock circuit comprises, an averaging circuit (Fig. 5, unit 15 performs claimed averaging; see paragraph [0076]) capable to output the phase adjust signal (Fig. 8, output of unit 15 is interpreted as claimed phase adjust signal)

in response to an average up signal, obtained from a plurality of up signals in a predetermined period of time, and an average down signal, obtained from a plurality of down signals, in the predetermined period of time (Paragraphs [0072]-[0077]).

Thus, it would have been obvious to a person of ordinary skill in the art to use the averaging circuit shown by Nakamura in the Chen's circuit because Nakamura's averaging circuit serves as a filter for blocking high-frequency components (Paragraph [0076])and hence prevents jitter characteristics from being lowered to generate high-quality clocks (Paragraph [0024]).

Allowable Subject Matter

4. Claims 2, 3, 7and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

4a. Regarding claim 2, prior art of record fails to show the circuit, wherein the clock circuit includes a phase adjust step-size logic capable of outputting an adjustable magnitude of the phase step-size in response to the variable data bit-rate, in combination with every other limitation of the claim and base claim.

4a. Regarding claim 3, prior art of record fails to show the circuit, wherein the phase adjust step-size logic is capable of outputting an adjustable direction of the phase step-size in response to the variable data bit-rate, in combination with every other limitation of the claim and base claim.

4a. Regarding claim 7, prior art of record fails to show the circuit, wherein the adjustable phase step-size is adjusted in response to a first step-size corresponding to data phase drift and a second step-size corresponding to the variable data bit-rate, in combination with every other limitation of the claim and base claim.

4a. Claim 8 is allowable as being dependent on claim 7.

5. Claims 10, 11, 14-24 and 30 are allowed.

The following is an examiner's statement of reasons for allowance:

5a. Regarding claim 10, prior art of record fails to show the circuit wherein the clock circuit includes a counter for obtaining a first step-size and the indicator provides a second step-size, wherein the first step size and the second step size are summed to obtain the adjustable phase step-size, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs. 1 and 7.

5b. Claim 11 is allowed as being dependent on claim 10.

5c. Regarding claim 14, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first

stage output signal in response to the data signal; a second stage, coupled to the first stage, capable a second stage output signal in response to the first of outputting stage output signal, a third stage, coupled to the second stage, capable outputting the phase adjust signal in response to the second stage output signal; and stall logic, coupled to the first, second and third stages, and capable of holding the phase adjust signal in response to the first and second stage output signals, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1 and 5.

5d. Claims 15-17 will be allowable as being dependent on claim 14.

5e. Regarding claim 18, prior art of record fails to show a circuit with a clock circuit comprising a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to the data signal; a second stage, coupled to the first stage, capable of outputting a second stage output signal in response to the first stage output signal; a third stage, coupled to the second stage, capable of outputting the phase adjust signal, having a first step-size, in response to the second stage output signal; stall logic, coupled to the first, second and third stages, capable of holding the phase adjust signal in response to the first and second stage output signals; an indicator, coupled to the third stage, capable of outputting a second step-size in response to the variable data bit- rate; and, a counter, coupled to the third stage and the indicator, capable of outputting the phase adjust signal having an adjustable step-size responsive to the first and

second step-sizes, in combination with every other limitation of the claim. The claim is interpreted in light of the specification, especially Figs 1, 5 and 7.

5f. Claims 19-24 will be allowable as being dependent on claim 18.

5g. Regarding claim 30, prior art of record fails to show a method for tracking signals wherein selecting an adjustable step-size includes determining a first step-size based on a variable data bit-rate of the signal; determining a second step-size and summing the first and second step sizes to obtain adjustable the step-size, in combination with each and every other limitation of the claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Contact Information

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vineeta S. Panwalkar whose telephone number is 571-272-8561. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/V. S. P./
Examiner, Art Unit 2611

/Mohammad H Ghayour/
Supervisory Patent Examiner, Art Unit 2611